

VN5025AJ-E

Single channel high side driver with analog sense for automotive applications

Features

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 to 36V
Max on-state resistance	R _{ON}	25 m Ω
Current limitation (typ)	I _{LIMH}	40 A
Off state supply current	IS	2 μΑ

General features

- Inrush current active management by power limitation
- Very low stand-by current
- 3.0V CMOS compatible input
- Optimized electromagnetic emission
- Very low electromagnetic susceptibility
- In compliance with the 2002/95/EC european directive

Diagnostic functions

- proportional load current sense
- high current sense precision for wide range currents
- current sense disable
- thermal shutdown indication
- very low current sense leakage

Protection

- Undervoltage shut-down
- Overvoltage clamp
- package
- Load current limitation
- Self limiting of fast thermal transients
- Protection against loss of ground and loss of $\mbox{V}_{\mbox{\scriptsize cc}}$
- Thermal shut down



- Reverse battery protection (see Application schematic)
- Electrostatic discharge protection

Application

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VN5025AJ-E is a monolithic device made using STMicroelectronics VIPower technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio) when CS DIS is driven low or left open. When CS DIS is driven high, the CURRENT SENSE pin is in a high impedance condition. Output current limitation protects the device in overload condition. In case of long overload duration, the device limits the dissipated power to safe level up to thermal shut-down intervention. Thermal shut-down with automatic restart allows the device to recover normal operation as soon as fault condition disappears.

Table 1. Device summary

	Package	Order codes			
	rackage	Tube	Tape and Reel		
	PowerSSO-12	VN5025AJ-E	VN5025AJTR-E		

Contents VN5025AJ-E

Contents

1	Bloc	k diagram and pin description	5
2	Elec	trical specifications	7
	2.1	Absolue maximum ratings	7
	2.2	Thermal data	8
	2.3	Electrical characteristics	9
	2.4	Electrical characteristics curves	8
3	Арр	lication information	1
	3.1	GND protection network against reverse battery 2	1
		3.1.1 Solution 1: resistor in the ground line (RGND only)	1
		3.1.2 Solution 2: a diode (DGND) in the ground line	2
	3.2	Load dump protection	2
	3.3	MCU I/Os protection	2
	3.4	Maximum demagnetization energy (VCC = 13.5V)	3
4	Pack	kage and PC board thermal data	4
	4.1	PowerSSO-12 TM thermal data	4
5	Pack	kage and packing information2	7
	5.1	ECOPACK® packages 2	7
	5.2	PowerSSO-12™ mechanical data 2	7
	5.3	Packing information 2	9
6	Revi	sion history	0

VN5025AJ-E List of tables

List of tables

Table 1.	Device summary	. 1
Table 2.	Pin function	. 5
Table 3.	Suggested connections for unused and N.C. pins	. 6
Table 4.	Absolute maximum ratings	. 7
Table 5.	Thermal data	. 8
Table 6.	Power section	. 9
Table 7.	Switching (VCC=13V, Tj=25°C)	10
Table 8.	Logic input	10
Table 9.	Protection and diagnostics	
Table 10.	Current sense (8V <v<sub>CC<16V)</v<sub>	11
Table 11.	Truth table	15
Table 12.	Electrical transient requirements	
Table 13.	Thermal parameter	26
Table 14.	PowerSSO-12 TM mechanical data	28
Table 15.	Document revision history	30

List of figures VN5025AJ-E

List of figures

Figure 1.	Block diagram	
Figure 2.	Configuration diagram (top view)	6
Figure 3.	Current and voltage conventions	7
Figure 4.	Current sense delay characteristics	
Figure 5.	Delay response time between rising edge of ouput current and rising edge of current sens	е
	(CS enabled)	13
Figure 6.	I _{OUT} /I _{SENSE} Vs. I _{OUT}	14
Figure 7.	Maximum current sense ratio drift vs load current- to update	14
Figure 8.	Switching characteristics	15
Figure 9.	Output voltage drop limitation	15
Figure 10.	Waveforms	
Figure 11.	Off state output current	18
Figure 12.	High level input current	
Figure 13.	Input clamp voltage	18
Figure 14.	Input low level	
Figure 15.	Input high level	
Figure 16.	Input hysteresis voltage	
Figure 17.	On state resistance vs. T _{case}	19
Figure 18.	On state resistance vs. V _{CC}	19
Figure 19.	Undervoltage shutdown	19
Figure 20.	Turn- On voltage slope	19
Figure 21.	I _{LIMH} vs. T _{case}	19
Figure 22.	Turn- Off voltage slope	19
Figure 23.	CS_DIS high level voltage	
Figure 24.	CS_DIS clamp voltage	
Figure 25.	CS_DIS low level voltage	
Figure 26.	Application schematic	
Figure 27.	Maximum turn Off current versus inductance	
Figure 28.	PowerSSO-12 TM PC board	
Figure 29.	Rthj-amb Vs. PCB copper area in open box free air condition	
Figure 30.	PowerSSO-12 TM thermal impedance junction ambient single pulse	25
Figure 31.	Thermal fitting model of a single channel HSD in PowerSSO-12 TM	25
Figure 32.	PowerSSO-12 [™] package dimensions	27
Figure 33.	PowerSSO-12 TM tube shipment (no suffix)	29
Figure 34.	PowerSSO-12 TM tape and reel shipment (suffix "TR"	29

1 Block diagram and pin description

Figure 1. Block diagram

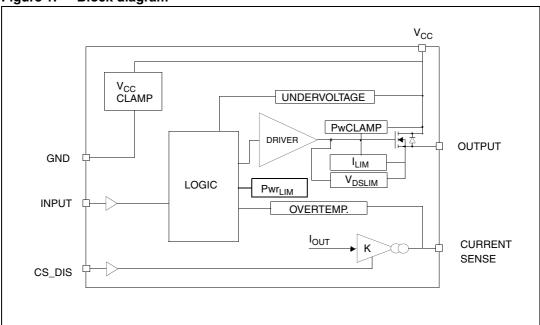


Table 2. Pin function

Name	Function
V _{CC}	Battery connection.
OUTPUT	Power output.
GND	Ground connection. Must be reverse battery protected by an external diode/resistor network.
INPUT	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state.
CURRENT SENSE	Analog current sense pin, delivers a current proportional to the load current.
CS_DIS	Active high CMOS compatible pin, to disable the current sense pin.

 $TAB = V_{CC}$ V_{cc} □ OUTPUT -12 11 GND OUTPUT 2 10 INPUT \square **OUTPUT** 3 ¦ 9 CURRENT_SENSE == OUTPUT 4 8 5 CS_DIS **OUTPUT** 7 6 V_{cc} OUTPUT

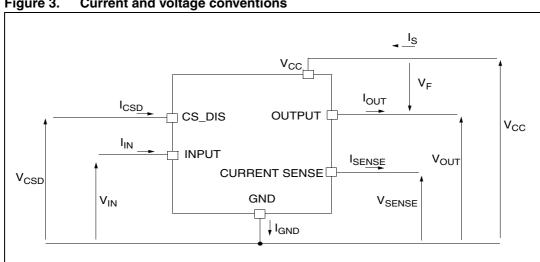
Figure 2. Configuration diagram (top view)

Table 3. Suggested connections for unused and N.C. pins

Connection / Pin	Current Sense	N.C.	Output	Input	CS_DIS
Floating	N.R. ⁽¹⁾	Х	Х	X	Х
To ground	Through 1kΩ resistor	Х	N.R.	Through 10kΩ resistor	Through 10kΩ resistor

^{1.} Not recommended.

2 **Electrical specifications**



Current and voltage conventions Figure 3.

Note:

 $V_F = V_{OUT} - V_{CC}$ during reverse battery condition.

Absolue maximum ratings 2.1

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to the conditions in table below for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality document.

Table 4. **Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V _{CC}	DC supply voltage	41	V
-V _{CC}	Reverse DC supply voltage	0.3	٧
- I _{GND}	DC reverse ground pin current	200	mA
I _{OUT}	DC output current	Internally limited	Α
- I _{OUT}	Reverse DC output current	24	Α
I _{IN}	DC input current	-1 to 10	mA
I _{CSD}	DC current sense disable input current	-1 to 10	mA
-I _{CSENSE}	DC reverse CS pin current	200	mA
V _{CSENSE}	Current Sense maximum voltage	V _{CC} -41 +V _{CC}	V V
E _{MAX}	Maximum switching energy (single pulse) (L=0.8mH; R_L =0Ω; V_{bat} =13.5V; T_{jstart} =150°C; I_{OUT} = I_{limL} ($Typ.$))	140	mJ

 Table 4.
 Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
	Electrostatic discharge (Human Body Model: R=1.5KΩ; C=100pF)		
	- INPUT	4000	V
V _{ESD}	- CURRENT SENSE	2000	V
	- CS_DIS	4000	V
	- OUTPUT	5000	V
	- V _{CC}	5000	V
V _{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T _j	Junction operating temperature	-40 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 5. Thermal data

Symbol	Parameter	Max Value	Unit
R _{thj-case}	Thermal resistance junction-case (MAX)	1.4	°C/W
R _{thj-amb}	Thermal resistance junction-ambient (MAX)	See Figure 29	°C/W

2.3 Electrical characteristics

The values specified in this section are for 8V<V $_{CC}$ <36V; -40°C<T $_{j}$ <150°C, unless otherwise stated.

Table 6. Power section

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{CC}	Operating supply voltage		4.5	13	36	V
V _{USD}	Undervoltage shutdown			3.5	4.5	V
V _{USDhyst}	Undervoltage shutdown hysteresis			0.5		V
R _{ON}	On State resistance	I _{OUT} = 3A; T _j = 25°C I _{OUT} = 3A; T _j = 150°C I _{OUT} = 3A; V _{CC} = 5V; T _j =25°C			25 50 35	$m\Omega$ $m\Omega$
V _{clamp}	Clamp voltage	I _S = 20 mA	41	46	52	V
I _S	Supply current	Off State; V_{CC} =13V; T_j =25°C; V_{IN} = V_{OUT} = V_{SENSE} = V_{CSD} =0V On State; V_{CC} =13V; V_{IN} =5V;		2 ⁽¹⁾	5 ⁽¹⁾	μΑ
		I _{OUT} = 0A		1.5	3	mA
I _{L(off)}	Off State output current	$V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 25^{\circ}C$ $V_{IN} = V_{OUT} = 0V; V_{CC} = 13V; T_j = 125^{\circ}C$	0 0	0.01	3 5	μΑ
V _F	Output - V _{CC} diode voltage	-l _{OUT} =4A; T _j =150°C			0.7	٧

^{1.} PowerMOS leakage included.

Table 7. Switching (V_{CC} =13V, T_j =25°C)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-On delay time	$R_L = 4.3\Omega$ (see <i>Figure 8.</i>)		30		μs
t _{d(off)}	Turn-Off delay time	$R_L = 4.3\Omega$ (see <i>Figure 8.</i>)		50		μs
(dV _{OUT} /dt) _{on}	Turn-On voltage slope	$R_L = 4.3\Omega$		See Figure 20		V/ µs
(dV _{OUT} /dt) _{off}	Turn-Off voltage slope	$R_L = 4.3\Omega$		See Figure 22		V/ µs
W _{ON}	Switching energy losses during twon	$R_L = 4.3\Omega$ (see <i>Figure 8</i>)		0.47		mJ
W _{OFF}	Switching energy losses during twoff	$R_L = 4.3\Omega$ (see <i>Figure 8</i>)		0.45		mJ

Table 8. Logic input

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{IL}	Input low level voltage				0.9	V
I _{IL}	Low level input current	V _{IN} = 0.9V	1			μΑ
V _{IH}	Input high level voltage		2.1			V
I _{IH}	High level input current	V _{IN} = 2.1V			10	μΑ
V _{I(hyst)}	Input hysteresis voltage		0.25			V
V _{ICL}	Input clamp voltage	I _{IN} = 1mA I _{IN} = -1mA	5.5	-0.7	7	V V
V _{CSDL}	CS_DIS low level voltage				0.9	V
I _{CSDL}	Low level CS_DIS current	V _{CSD} = 0.9V	1			μΑ
V _{CSDH}	CS_DIS high level voltage		2.1			V
I _{CSDH}	High level CS_DIS current	V _{CSD} = 2.1V			10	μΑ
V _{CSD(hyst)}	CS_DIS hysteresis voltage		0.25			V
V _{CSCL}	CS_DIS clamp voltage	I _{CSD} =1mA I _{CSD} = -1mA	5.5	-0.7	7	V V

Table 9. Protection and diagnostics⁽¹⁾

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{limH}	DC short circuit current	V_{CC} = 13V 5V< V_{CC} <36V	28	40	56 56	A A
I _{limL}	Short circuit current during thermal cycling	V_{CC} = 13V; $T_R < T_j < T_{TSD}$		16		Α
T _{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T _{RS} + 1	T _{RS} + 5		°C
T _{RS}	Thermal reset of STATUS		135			°C
T _{HYST}	Thermal hysteresis (T _{TSD} -T _R)			7		°C
V _{DEMAG}	Turn-Off output voltage clamp	I _{OUT} = 2A; V _{IN} =0; L=6mH	V _{CC} -41	V _{CC} -46	V _{CC} -52	V
V _{ON}	Output voltage drop limitation	I_{OUT} = 0.2A T_j = -40°C150°C (see <i>Figure 9</i>)		25		mV

To ensure long term reliability under heavy overload or short circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device operates under abnormal conditions this software must limit the duration and number of activation cycles.

Table 10. Current sense (8V<V_{CC}<16V)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
K _{LED}	lout/Isense	I_{OUT} = 0.05A, V_{SENSE} =0.5V, V_{CSD} =0V T_{j} = -40°C150°C	1420	3420	5180	
К ₀	lout/lsense	I _{OUT} = 0.5A; V _{SENSE} =0.5V; V _{CSD} =0V; T _j = -40°C150°C	2010	3100	4160	
$dK_0/K_0^{(1)}$	Current Sense ratio drift	I _{OUT} =0.5 A; V _{SENSE} = 0.5 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-12		12	%
К ₁	lout/Isense	I _{OUT} = 2A; V _{SENSE} =4V; V _{CSD} =0V; T _j = -40°C150°C T _j = 25°C150°C	2220 2310	2880 2880	3600 3450	
dK ₁ /K ₁ ⁽¹⁾	Current Sense ratio drift	I _{OUT} =2A; V _{SENSE} = 4V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-10		10	%
K ₂	lout/Isense	I _{OUT} = 3A; V _{SENSE} =4V; V _{CSD} =0V; T _j = -40°C150°C T _j = 25°C150°C	2380 2490	2870 2870	3400 3250	

Table 10. Current sense (8V<V_{CC}<16V) (continued)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
dK ₂ /K ₂ ⁽¹⁾	Current Sense ratio drift	I _{OUT} =3 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-7		7	%
К ₃	lout/Isense	I _{OUT} = 10A; V _{SENSE} =4V; V _{CSD} =0V; T _j = -40°C150°C T _j =25°C150°C	2700 2700	2860 2860	3050 3050	
$dK_3/K_3^{(1)}$	Current Sense ratio drift	I _{OUT} = 10 A; V _{SENSE} = 4 V; V _{CSD} =0V; T _J = -40 °C to 150 °C	-4		4	%
I _{SENSE0}	Analog Sense leakage current	I _{OUT} =0A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =0V; T _j =-40°C150°C V _{CSD} =0V; V _{IN} =5V; T _j =-40°C150°C I _{OUT} =2A; V _{SENSE} =0V; V _{CSD} =5V; V _{IN} =5V; T _j =-40°C150°C	0 0		1 2 1	μ Α μ Α μ Α
l _{OL}	Openload On state current detection threshold	V _{IN} = 5V, I _{SENSE} = 5 μA	5		30	mA
V _{SENSE}	Max analog Sense output voltage	I _{OUT} =3A; V _{CSD} =0V	5			٧
V _{SENSEH}	Analog Sense output voltage in overtemperature condition	V_{CC} =13V; R_{SENSE} =3.9K Ω		9		٧
I _{SENSEH}	Analog Sense output current in overtemperature condition	V _{CC} =13V; V _{SENSE} =5V		8		mA
t _{DSENSE1H}	Delay response time from falling edge of CS_DIS pin	V _{SENSE} <4V, 0.5 <lout<10a I_{SENSE}=90% of I_{SENSE max} (see <i>Figure 4</i>)</lout<10a 		50	100	μs
t _{DSENSE1L}	Delay response time from rising edge of CS_DIS pin	V _{SENSE} <4V, 0.5 <lout<10a I_{SENSE}=10% of I_{SENSE max} (see <i>Figure 4</i>)</lout<10a 		5	20	μs
t _{DSENSE2H}	Delay response time from rising edge of INPUT pin	V _{SENSE} <4V, 0.5 <lout<10a I_{SENSE}=90% of I_{SENSE max} (see <i>Figure 4</i>)</lout<10a 		70	300	μs

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Δt _{DSENSE2} H	Delay response time between rising edge of output current and rising edge of current sense	V _{SENSE} < 4V, I _{SENSE} = 90% of I _{SENSEMAX} , I _{OUT} = 90% of I _{OUTMAX} I _{OUTMAX} = 5A (see <i>Figure 5</i>)			130	μs
t _{DSENSE2L}	Delay response time from falling edge of	V _{SENSE} <4V, 0.5 <lout<10a I_{SENSE}=10% of I_{SENSE} max</lout<10a 		100	250	μs

Table 10. Current sense (8V<V_{CC}<16V) (continued)

t_{DSENSE2H}

INPUT pin



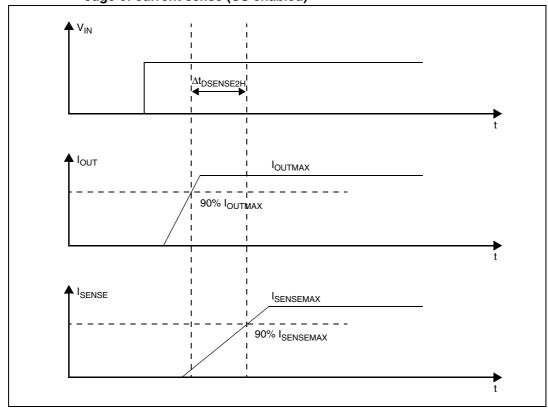
t_{DSENSE1H}

t_{DSENSE2L}

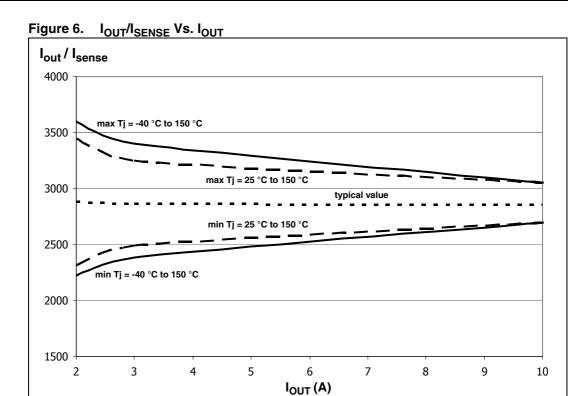
(see Figure 4)

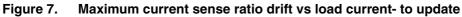
Figure 5. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

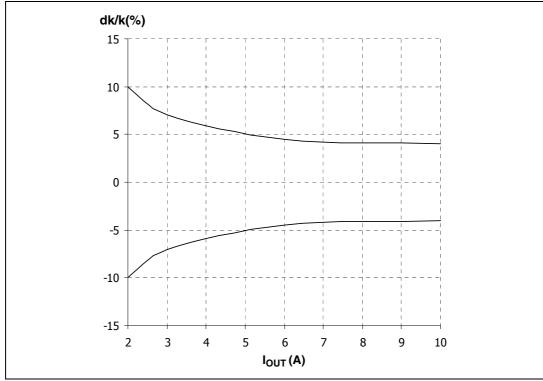
t_{DSENSE1L}



^{1.} Parameter guaranteed by design, it is not tested.







Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	Sense (V _{CSD} =0V) ⁽¹⁾
Normal operation	L	L	0
Normai operation	Н	Н	Nominal
Overtemperature	L	L	0
Overtemperature	Н	L	V _{SENSEH}
Lindonyoltogo	L	L	0
Undervoltage	Н	L	0
Short circuit to GND	L	L	0
(Rsc ≤10 mΩ)	Н	L	0 if $T_j < T_{TSD}$
Chart aircuit to V	L	Н	0
Short circuit to V _{CC}	Н	Н	< Nominal
Negative output voltage clamp	L	L	0

^{1.} If the V_{CSD} is high, the SENSE output is at a high impedance, its potential depends on leakage currents and external circuit.

Figure 8. Switching characteristics

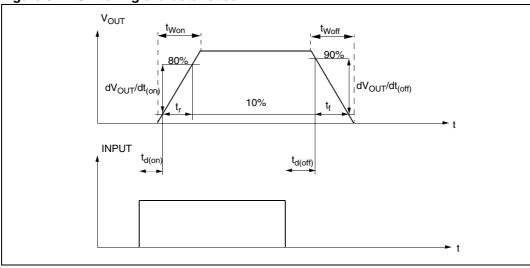


Figure 9. Output voltage drop limitation

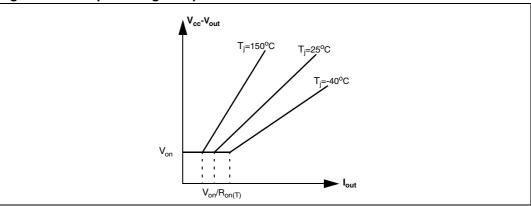


Table 12. Electrical transient requirements

ISO 7637-2: 2004(E)	Test le	Test levels ⁽¹⁾		Burst cy	Delays and	
Test pulse	III	IV	pulses or test times	repetition time imp		impedance
1	-75V	-100V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37V	+50V	5000 pulses	0.2 s	5 s	50 μs, 2 Ω
3a	-100V	-150V	1h	90 ms	100 ms	0.1 μs, 50 Ω
3b	+75V	+100V	1h	90 ms	100 ms	0.1 μs, 50 Ω
4	-6V	-7V	1 pulse			100 ms, 0.01 Ω
5b ⁽²⁾	+65V	+87V	1 pulse			400 ms, 2 Ω

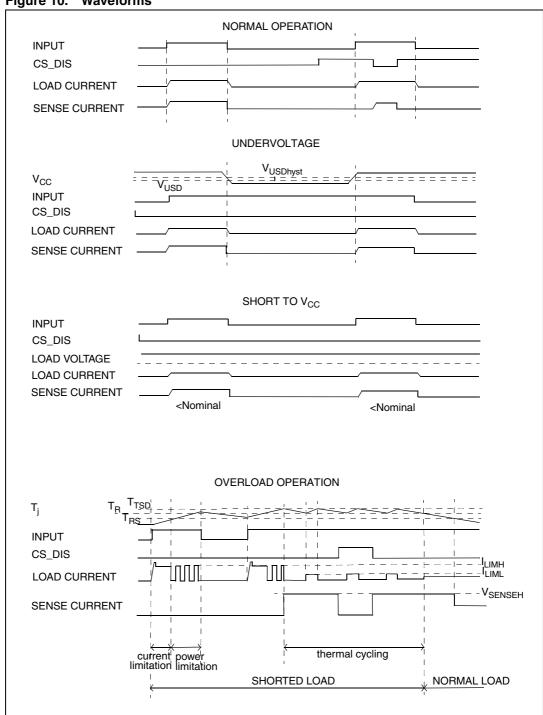
ISO 7637-2: 2004(E)	Test level	results ⁽¹⁾
Test pulse	III	IV
1	С	С
2	С	С
3a	С	С
3b	С	С
4	С	С
5 ⁽²⁾	С	С

^{1.} The above test levels must be considered referred to Vcc = 13.5V except for pulse 5b.

^{2.} Valid in case of external load dump clamp: 40V maximum referred to ground.

Class	Contents
С	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

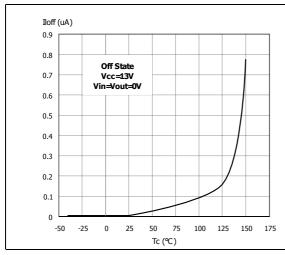
Figure 10. Waveforms



2.4 Electrical characteristics curves

Figure 11. Off state output current

Figure 12. High level input current



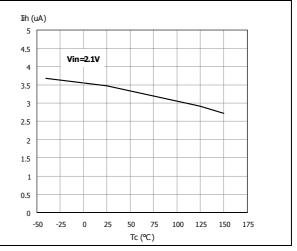
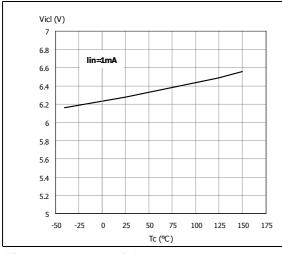


Figure 13. Input clamp voltage

Figure 14. Input low level



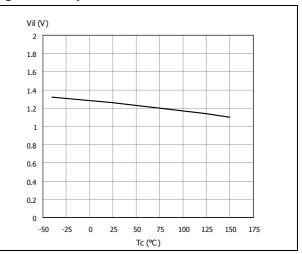
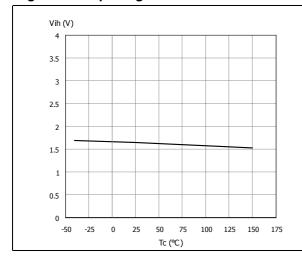
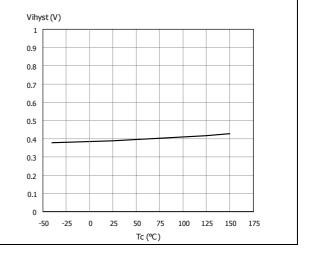


Figure 15. Input high level

Figure 16. Input hysteresis voltage

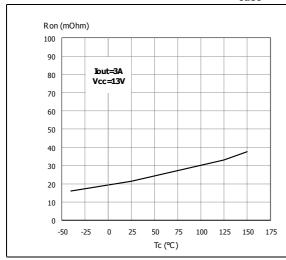




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Figure 17. On state resistance vs. T_{case}

Figure 18. On state resistance vs. V_{CC}



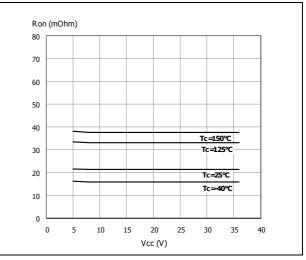
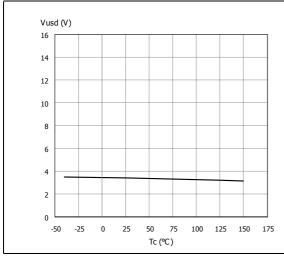


Figure 19. Undervoltage shutdown

Figure 20. Turn- On voltage slope



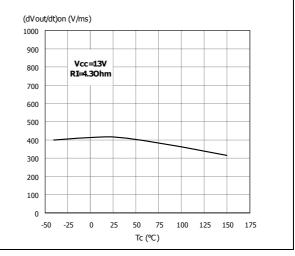
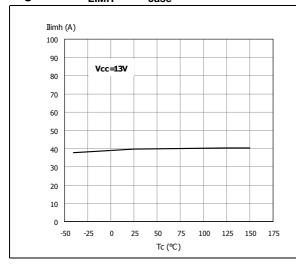


Figure 21. I_{LIMH} vs. T_{case}

Figure 22. Turn- Off voltage slope



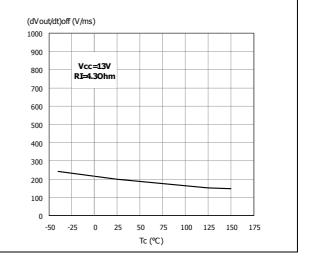
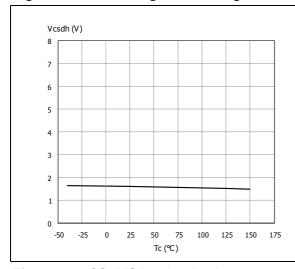


Figure 23. CS_DIS high level voltage

Figure 24. CS_DIS clamp voltage



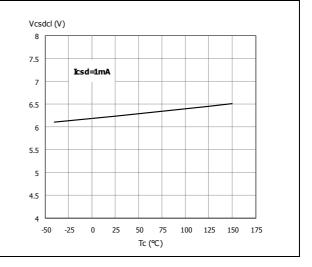
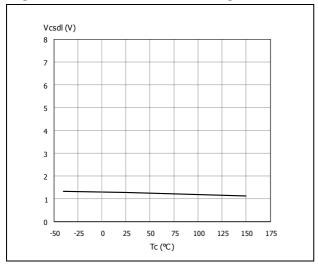
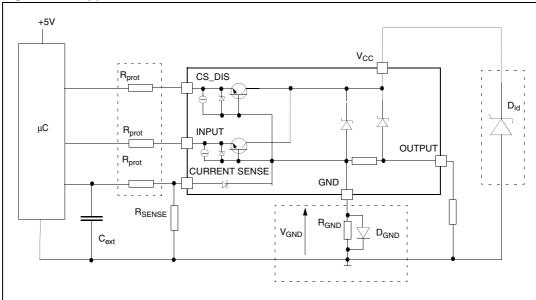


Figure 25. CS_DIS low level voltage



3 Application information

Figure 26. Application schematic



3.1 GND protection network against reverse battery

3.1.1 Solution 1: resistor in the ground line (R_{GND} only)

This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

- 1. $R_{GND} \leq 600 \text{mV} / (I_{S(on)max})$.
- 2. $R_{GND} \ge (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device datasheet.

Power Dissipation in R_{GND} (when V_{CC} <0: during reverse battery situations) is:

$$P_{D} = (-V_{CC})^2 / R_{GND}$$

This resistor can be shared amongst several different HSDs. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not shared by the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND} .

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then ST suggests to utilize Solution 2 (see below).

3.1.2 Solution 2: a diode (D_{GND}) in the ground line

A resistor (R_{GND} =1k Ω) should be inserted in parallel to D_{GND} if the device drives an inductive load.

This small signal diode can be safely shared amongst several different HSDs. Also in this case, the presence of the ground network will produce a shift ($\approx 600 \text{mV}$) in the input threshold and in the status output values if the microprocessor ground is not common to the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

3.2 Load dump protection

 D_{ld} is necessary (Voltage Transient Suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2: 2004(E) table.

3.3 MCU I/Os protection

If a ground protection network is used and negative transient are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the μC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of μC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of μC I/Os.

-V_{CCpeak}/I_{latchup} ≤R_{prot} ≤(V_{OHµC}-V_{IH}-V_{GND}) / I_{IHmax}

Calculation example:

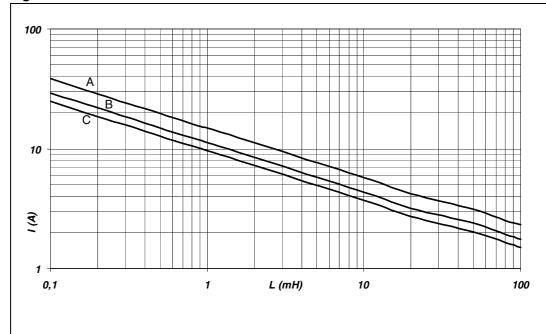
For V_{CCpeak} = - 100V and $I_{latchup} \ge 20mA$; $V_{OH\mu C} \ge 4.5V$

 $5k\Omega \le R_{prot} \le 180k\Omega$

Recommended values: $R_{prot} = 10k\Omega$, $C_{EXT} = 10nF$.

3.4 Maximum demagnetization energy ($V_{CC} = 13.5V$)

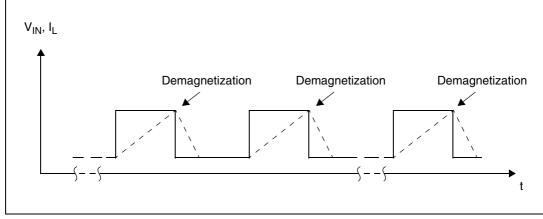
Figure 27. Maximum turn Off current versus inductance



A: $T_{jstart} = 150^{\circ}C$ single pulse

B: T_{istart} = 100°C repetitive pulse

C: T_{istart} = 125°C repetitive pulse



Note:

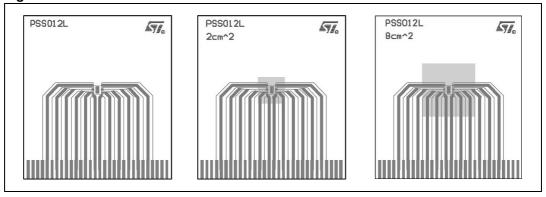
Values are generated with $R_L = 0\Omega$

In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 PowerSSO-12™ thermal data

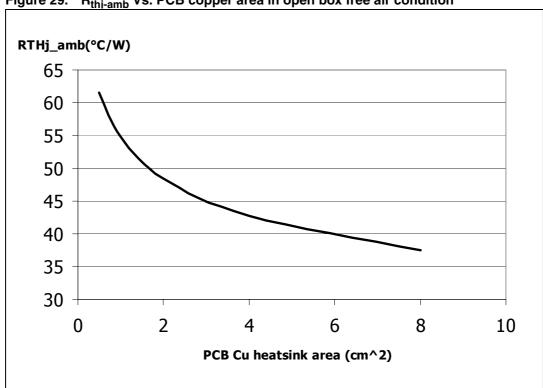
Figure 28. PowerSSO-12[™] PC board



Note:

Layout condition of R_{th} and Z_{th} measurements (PCB: Double layer, Thermal Vias, FR4 area= 77mm x 86mm, PCB thickness=1.6mm, Cu thickness=70 μ m (front and back side), Copper areas: from minimum pad lay-out to 8cm²).

Figure 29. R_{thi-amb} Vs. PCB copper area in open box free air condition



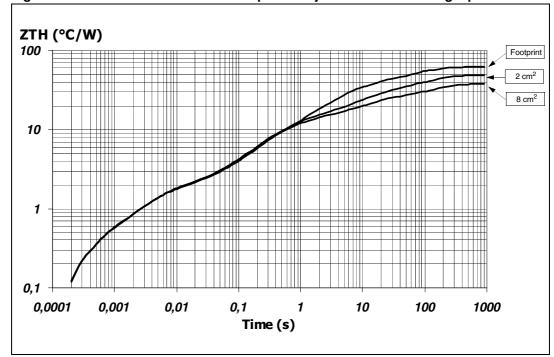
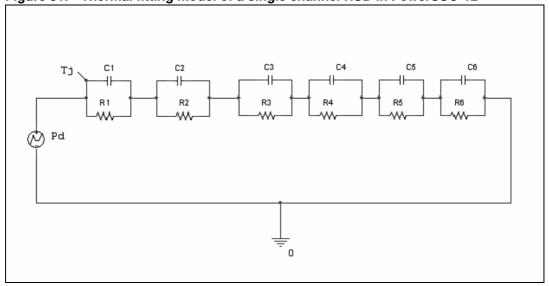


Figure 30. PowerSSO-12[™] thermal impedance junction ambient single pulse

Figure 31. Thermal fitting model of a single channel HSD in PowerSSO-12™



Equation 1: pulse calculation formula:

$$\begin{split} Z_{TH\delta} &= R_{TH} \cdot ~\delta + Z_{THtp} (1 - \delta) \\ \text{where} ~~\delta &= t_p / ~T \end{split}$$

Table 13. Thermal parameter

Area/island (cm ²)	Footprint	2	8
R1 (°C/W)	0.3		
R2 (°C/W)	1.3		
R3 (°C/W)	4		
R4 (°C/W)	8	8	7
R5 (°C/W)	22	15	10
R6 (°C/W)	26	20	15
C1 (W.s/°C)	0.001		
C2 (W.s/°C)	0.003		
C3 (W.s/°C)	0.05		
C4 (W.s/°C)	0.2	0.1	0.1
C5 (W.s/°C)	0.27	0.8	1
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK® packages

In order to meet environmental requirements, ST offers these devices in ECOPACK[®] packages. ECOPACK[®] packages are lead-free. The category of Second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at www.st.com.

5.2 PowerSSO-12™ mechanical data

hx45'

B

SEATING
PLANE

0,25 mm
GAUGE PLANE

Figure 32. PowerSSO-12™ package dimensions

Table 14. PowerSSO-12[™] mechanical data

Dimension _		Millimeters	
Dimension	Min.	Тур.	Max.
А	1.250		1.620
A1	0.000		0.100
A2	1.100		1.650
В	0.230		0.410
С	0.190		0.250
D	4.800		5.000
E	3.800		4.000
е		0.800	
Н	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	Oº		8º
X	1.900		2.500
Υ	3.600		4.200
ddd			0.100

5.3 Packing information

Figure 33. PowerSSO-12[™] tube shipment (no suffix)

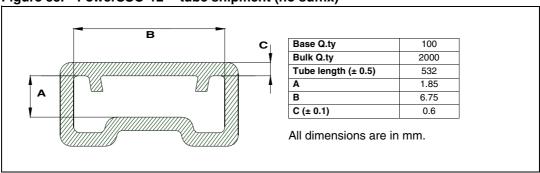
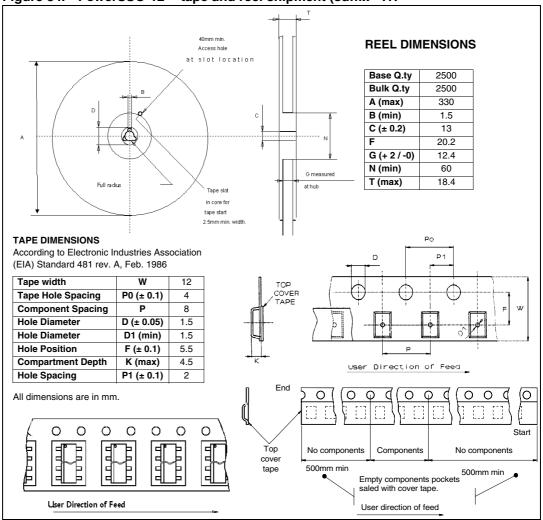


Figure 34. PowerSSO-12[™] tape and reel shipment (suffix "TR"



Revision history VN5025AJ-E

6 Revision history

Table 15. Document revision history

Date	Revision	Changes
12th-Jan-2004	1	Initial release.
17th-May-2006	2	Second release.
1st-Mar-2007	3	Added Contents, List of tables and List of figures. Added Section 3.4: Maximum demagnetization energy (VCC = 13.5V). Added ECOPACK® package information.
13-Dec-2007	4	Document reformatted and restructured. Table 4: Absolute maximum ratings: corrected E _{MAX} value from 90 to 140 mJ. Added Figure 5: Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled). Updated Figure 6: I _{OUT} /I _{SENSE} Vs. I _{OUT} . Added Figure 7: Maximum current sense ratio drift vs load current-to update. Table 10: Current sense (8V <v<sub>CC<16V): - added dk0/k0, dk1/k1, dk2/k2, dk3/k3, \(Distangle Lighting Light</v<sub>
12-Feb-2008	5	Corrected typing error in <i>Table 10: Current sense (8V<v<sub>CC<16V)</v<sub></i> : changed I_{OL} test condition from $V_{IN} = 0V$ to $V_{IN} = 5V$.

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